IN THE CLAIMS:

The following is a list of all claims including claims that have not been amended in the present response to Office Action.

Please replace claims 1, 3, 6 and 10 with the following claims 1, 3, 6 and 10, respectively.

1. (Once amended) In a method for designing a circuit where design parameters for performance specifications are represented by posynomial expressions with constraints and solved with geometric programming, an improvement for simultaneously determining the boundaries for circuit elements in the floorplan of the circuit comprising:

representing the boundaries for circuit elements in the floorplan of the circuit as posynomial expressions with constraints on circuit size;

simultaneously solving the posynomial expressions for the design parameters and solving the posynomial expressions for the floorplan boundaries on a digital computer using geometric programming;

outputting the results in a format that can be used by a circuit designer in the fabrication of the circuit.

2. The method defined by claims 1 wherein the representation of the floorplan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements.

3. (once amended) The method defined by claim 1 including using layout constraints for the floorplan.

4. The method defined by claim 3 wherein one layout constraint is a limitation on the circuit area.

5. The method defined by claim 4 wherein another layout constraint is a limitation on the aspect ratio of the circuit layout.

6. (once amended) In a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, an improvement for simultaneously determining the boundaries for the active circuit elements in a floorplan for the integrated circuit comprising:

representing the floorplan as posynomial constraints of vertical and horizontal dimensions for regions where the active circuit elements are placed;

simultaneously solving the posynomial expressions for the design parameters and the posynomial constraints for the vertical and horizontal dimensions; and

outputting the results of the preceding step in a format usable for a circuit designer to fabricate the integrated circuit.

7. The method defined by claim 6 wherein the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements.

8. The method defined by claim 7 wherein for a vertical slice, the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which

dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node.

9. The method defined by claim 8 wherein for each horizontal slice, the resulting second sibling nodes are represented by the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node.

A4 Cl

10. (once amended) The method defined by claim 9 wherein the circuit elements include MOS transistors where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression.

11. The method defined by claim 10 wherein the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters.

12. The method defined by claim defined by claim 11 wherein the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions.

Please add new claims 13 through 24.

B A5 Cl

13. (new) A ~~machine~~ computer readable medium having stored thereon instructions which when executed by a processor cause the processor to perform in a method for designing a circuit where design parameters for performance

specifications are represented by posynomial expressions with constraints and solved with geometric programming and for simultaneously determining the boundaries for circuit elements in the floorplan of the circuit, the method comprising:

simultaneously solving the posynomial expressions for the design parameters of the circuit and solving posynomial expressions for the floorplan boundaries of the circuit elements using geometric programming, the posynomial expressions for the floorplan boundaries represented as constraints on circuit size;

outputting the results in a format that can be used by a circuit designer in the fabrication of the circuit.

14. (new) The ~~machine~~ computer readable medium defined by claims 13 wherein the representation of the floorplan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements.

15. (new) The ~~machine~~ computer readable medium defined by claim 13 including using layout constraints for the floorplan.

16. (new) The ~~machine~~ computer readable medium defined by claim 15 wherein one layout constraint is a limitation on the circuit area.

17. (new) The ~~machine~~ computer readable medium defined by claim 16 wherein another layout constraint is a limitation on the aspect ratio of the circuit layout.

18. (new) A ~~machine~~ computer readable medium having stored thereon instructions which when executed by a processor cause the processor to perform a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, and for simultaneously determining the boundaries for the active circuit elements in a floorplan for the integrated circuit, the method comprising:

representing the floorplan as posynomial constraints of vertical and horizontal dimensions for regions where the active circuit elements are placed;

simultaneously solving the posynomial expressions for the design parameters and the posynomial constraints for the vertical and horizontal dimensions; and

outputting the results of the preceding step in a format usable for a circuit designer to fabricate the integrated circuit.

19. (new) The ~~machine~~ computer readable medium defined by claim 18 wherein the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements.

20. (new) The ~~machine~~ Computer readable medium defined by claim 19 wherein for a vertical slice, the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node.

21. (new) The ~~machine~~ Computer readable medium defined by claim 20 wherein for each horizontal slice, the resulting second sibling nodes are represented by

the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node.

22. (new) The ~~machine~~ computer readable medium defined by claim 18 wherein the circuit elements include MOS transistors where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression.

23. (new) The ~~machine~~ computer readable medium defined by claim 22 wherein the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters.

24. (new) The ~~machine~~ computer readable medium defined by claim 23 wherein the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions.

COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on August 7, 2002. At the time the Examiner mailed the Office Action, claims 1 through 12 were pending. In response, the Applicant has: 1) added new claims 13 through 24; 2) has amended claims 1, 3, 6 and 10; and, 3) has not canceled any claims. As such, claims 1 through 24 are currently pending. The Applicant respectfully requests reconsideration of the present application and the allowance of claims 1 through 24.

The Examiner has objected to claim 10 under 37 CFR 1.75(c) as being in improper in form because of its multiple dependency. In response the Applicant has amended claim 10 so as to depend from claim 9. As such, the multiple dependent form of claim 10 has been removed; and, as a consequence, the Examiner's objection has been overcome.

The Examiner has rejected each of independent claims 1 through 12 under 35 USC 102(e) as being anticipated by U.S. Patent No. 6,209,119 (hereinafter "Fukui"). "To anticipate a claim, the reference must teach every element of the claim" MPEP 2131. The Applicant respectfully submits that Fukui fails to disclose each and every element of the Applicant's independent claims 1 and 6; and, therefore is insufficient to anticipate these claims.

Fukui discloses a method and apparatus for the automated design of digital circuits where some form of geometric programming is utilized in order to

provide circuit designers, at a high level description environment for their circuit, specific power consumption and delay details. Fukui is aimed at providing designers with this information at a high level (e.g., HDL, RTL) so that timing problems/issues are discovered and corrected for prior to the circuit being fully translated into lower levels of detail (e.g., gate/logic level, transistor level). Here, the Background of Fukui is illustrative:

> "[T]he capability to correct the result of the upper process of the design in the lower process of the design (logic level and transistor level) becomes extremely important. By establishing a close linkage between the evaluating capability in the upper process of design and the correcting capability in the lower process of design, iteration in the LSI design can be lessened, which reduces design cost and implements higher-quality LSI design.
> To Establish a close linkage between the upper and lower processes of design, it is necessary to provide, from the lower side of design, accurate data about the performance and area of a module required by the upper side of design in a shorter period of time."

Fukui, Column 1, lines 30-42.

As such, Fukui is directed to the production of a "layout module" and "estimation information" that can be used at a high level of detail to describe a logic circuit path; yet, includes or otherwise takes account of details traditionally reserved for lower levels of detail (e.g., delay). With what is effectively *a priori* knowledge of finer circuit details during the high level design description process, costly "re-designs" (e.g., associated with the "discovery" of timing problems) only after the circuit has been fully compiled into a lower level of detail is avoided.

As various aspects of Fukui involve some degree of geometric programming; and, as the Applicant's claims are directed to geometric programming, it is important to clearly bring forward exactly what details of Fukui actually apply to Applicant's claims. Applicant's claims presently claim the *simultaneous* solving of posynomial expressions for circuit performance specifications and posynomial expressions for circuit layout. The Applicant respectfully submits that such detail is lacking in Fukui.

In particular, note that Figure 15 of Fukui presents a depiction of a complete process for generating both the aforementioned "layout module" and the "estimation data". Apparently, geometric programming where an optimization problem is actually solved only comes into play in two separate instances over the course of executing the method that is observed in Figure 15 of Fukui.

A first instance occurs at step ST8 where "the transistor-level-driving-ability optimizing unit 38 performs for each cell specified in step ST7, optimization of the in-cell driving ability and layout synthesis in order to minimize in-cell delay and area." Column 12, lines 12-15. Note that "[t]he transistor level driving ability optimizing unit 38 optimizes the size of each transistor within each cell such that the area occupied by the transistors is minimized when the transistor size in the output stage of the cell and a delay time of the cell are specified. The optimization is implemented by using, for example, a method of optimizing a transistor size disclosed in "TILOS: A Posynomial Programming Approach to Transistor Sizing" (Fishburn et. al. ICCADDR85, pp. 326-328, 1985)." Column

11, lines 5-13. The Applicant respectfully submits that these statements of Fukui do not disclose the simultaneous solving of posynomial expressions for circuit performance specifications and posynomial expressions for circuit layout.

A second instance occurs at step ST10, where, "[b]ased on the output-stage driving ability and in cell-delay requirement of each cell, the cell property estimating unit 32 obtains, for each cell, the geometrical function parameterized by delay." Column 12, lines 29-32. Note that a more thorough discussion of the operation of the cell property estimating unit 32 is described from Column 8 line 1 to Column 10, line 29. Here, the only mention of geometric problem solving with respect to the operation of the cell property estimating unit 32 is provided with respect to "Step E2" where "[a] gate width of each transistor is optimized (by appropriately using a method of optimizing a transistor size disclosed, for example, in TILOS: A Posynomial Programming Approach to Transistor Sizing" (Fishburn et. al. ICCADDR85, pp. 326-328, 1985)." The Applicant respectfully submits that these statements (or any of the previous cited statements) of Fukui do not disclose the simultaneous solving of posynomial expressions for circuit performance specifications and posynomial expressions for circuit layout.

Moreover, no where else does Fukui discuss geometric programming in the sense that a geometric optimization problem is actually solved. As such, no other discussions within Fukui could disclose the simultaneous solving of posynomial expressions for circuit performance specifications and posynomial expressions for circuit layout.

As such, each ofindependent claims 1 and 6 are patentable over Fukui. For similar reasons new independent claims 13 and 18 are also patentable over Fukui.

For at least these reasons, the Applicant respectfully requests the allowance of claims 1 through 24.

As such, believing claims 1 through 16 to have overcome all existing rejections and objections, applicant respectfully requests allowance of same.